DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Winter Examination – 2025

Course: B.Tech. **Branch : Electronics & Telecomm Engineering** **Semester : III**

Subject Code & Name: 25AF1372PC303/25AF1376PC303_Digital Electronics

Max Marks: 60 **Date:31/01/2026** **Duration: 3 Hr.**

Instructions to the Students:

1. *Each question carries 12 marks.*
2. *Question No. 1 will be compulsory and include objective-type questions.*
3. *Candidates are required to attempt any four questions from Question No. 2 to Question No. 6.*
4. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
5. *Use of non-programmable scientific calculators is allowed.*
6. *Assume suitable data wherever necessary and mention it clearly.*

		(Level /CO)	Marks
Q. 1	**Objective type questions. (Compulsory Question)**		**12**
1	Fan-out refers to a) Number of inputs of a gate b) Number of outputs c) Number of gates driven by output d) Power dissipation	**CO 3**	**1**
2	Behavioral modeling in VHDL describes a) Hardware structure b) Data flow only c) Functionality of circuit d) Physical layout	**CO 3**	**1**
3	T flip-flop toggles when a) T = 0 b) T = 1 c) Clock = 0 d) Preset = 1	**CO 3**	**1**
4	The invalid condition in SR flip-flop occurs when a) S=0, R=0 b) S=1, R=0 c) S=0, R=1 d) S=1, R=1	**CO 4**	**1**
5	POS representation of a logic function uses a) Minterms b) Maxterms c) Literals only d) XOR gates	**CO 4**	**1**
6	A 1-bit memory cell can store a) No information b) One binary digit c) Two binary digits d) Decimal digit	**CO 4**	**1**
7	Tri-state logic has a) Two output states b) Three output states c) Four output states d) No output	**CO 4**	**1**
8	Ring counter is a type of a) Asynchronous counter b) Synchronous counter c) Shift register counter d) Up-down counter	**CO 2**	**1**
9	TTL logic uses a) MOSFETs b) BJTs c) JFETs d) SCRs	**CO 4**	**1**
10	Moore machine output depends on a) Input only b) Present state only c) Next state only d) Clock only	**CO 4**	**1**
11	Don’t care conditions in K-map are used to a) Increase gate count b) Reduce logic complexity c) Avoid simplification d) Increase power dissipation	**CO 4**	**1**

12	Multiplexer is a circuit that a) Selects one input from many b) Converts code c) Stores data d) Compares numbers	**CO 2**	**1**

Q. 2	**Solve the following.**		**12**
A)	Convert the following Boolean expression into Standard SOP & POS form $F = B.\overline{C} + A + A.\overline{B}.C$	**CO 1**	**6**
B)	Minimize the Boolean function using K-map and implement simplified output using logic gates. **F(A,B,C,D) = Σm(0,2,3,7,8,10,11,15) + d (4,9,14)**	**CO 2**	**6**

Q.3	**Solve the following.**		**12**
A)	Design a **Mealy sequence detector** for detecting **1101 using T flipflop.**	**CO 2**	**6**
B)	Prepare a comparison table of **TTL, CMOS, ECL**.	**CO 2**	**6**

Q. 4	**Solve Any Two of the following.**		**12**
A)	Design 5:32 decoder using 3:8 decoder.	**CO 3**	**6**
B)	Draw and Explain Universal Shift Register.	**CO 3**	**6**
C)	Define **clock skew and clock jitter**. Explain their effects on sequential circuits.	**CO 4**	**6**

Q.5	**Solve Any Two of the following.**		**12**
A)	Implement following Boolean function using 2:1. $F = B.\overline{C} + A + A.\overline{B}.C$	**CO 3**	**6**
B)	Design a **4-bit synchronous up counter** using T flip-flops.	**CO 4**	**6**
C)	Describe general architecture of **FPGA.**	**CO 2**	**6**

Q. 6	**Solve Any Two of the following.**		**12**
A)	What are the five elements of VHDL?	**CO 2**	**6**
B)	Explain the **operation of TTL NAND gate** with neat diagram.	**CO 2**	**6**
C)	Write comparison between PLD types?	**CO 2**	**6**

***** End *****